

Appl. No. 10/051,535
Amdt. Dated December 27, 2005
Reply to Office action of August 4, 2005

IN THE CLAIMS

Please amend Claims 1-19 as follows:

The following marked up listing of claims replaces all prior versions, and listings, of claims in the application:

Marked Up Listing of Claims

1. (Currently Amended) A storage medium that provides software that, if executed by a computing device, will cause the computing device to perform the following operations ~~A method to efficiently design and implement a matched instruction set processor system, including:~~

~~analyzing and mapping~~ analyze and map design specifications of the matched instruction set processor into application components, each application component representing a reusable function commonly used in digital communication systems;

~~decomposing~~ decompose the matched instruction set processor system into interconnected design vectors; and

~~analyzing and mapping~~ analyze and map the interconnected design vectors into specific hardware and software elements.

2. (Currently Amended) The storage medium of claim 1, wherein the operation to analyze and map design specifications further comprises ~~The method of claim 1, wherein analyzing and mapping design specifications further includes:~~

~~performing~~ perform a behavioral analysis of the matched instruction set processor system to ensure compliance with the design specifications.

3. (Currently Amended) The storage medium of claim 1, wherein the operation to analyze and map design specifications further comprises ~~The method of claim 1, wherein analyzing and mapping design specifications further includes:~~

~~performing~~ perform a requirement analysis of the design specifications of the matched instruction set processor system to generate a behavioral model; and

~~representing~~ represent the behavioral model using application components.

4. (Currently Amended) The storage medium of claim 1, wherein the operation to decompose the matched instruction set processor system into interconnected design

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vectors further comprises ~~The method of claim 1, wherein decomposing the matched instruction set processor system into interconnected design vectors further includes:~~

~~mapping map~~ the application components into corresponding architectural components.

5. (Currently Amended) The storage medium of claim 4, wherein the operation to decompose the matched instruction set processor system into interconnected design vectors further comprises ~~The method of claim 4, wherein decomposing the matched instruction set processor system into interconnected design vectors further includes:~~

~~decomposing~~ decompose each application component into processing pipelines to satisfy system processing and timing requirements.

6. (Currently Amended) The storage medium of claim 5, wherein the operation to decompose the matched instruction set processor system into interconnected design vectors further comprises ~~The method of claim 5, wherein decomposing the matched instruction set processor system into interconnected design vectors further includes:~~

~~decomposing~~ decompose each processing pipeline into design vectors, including functional design vectors and interconnect design vectors.

7. (Currently Amended) The storage medium of claim 6, wherein the operation to decompose the matched instruction set processor system into interconnected design vectors further comprises ~~The method of claim 6, wherein decomposing the matched instruction set processor system into interconnected design vectors further includes:~~

[[using]] use the functional design vectors to represent design information for at least one functional aspect of the processing pipeline; and

[[using]] use the interconnect design vectors to contain connectivity characteristics of the processing pipeline.

8. (Currently Amended) The storage medium of claim 6, wherein the operation to decompose the matched instruction set processor system into interconnected design vectors further comprises ~~The method of claim 7, wherein decomposing the matched instruction set processor system into interconnected design vectors further includes:~~

~~providing~~ provide in each design vector a binding header method, a run method, a conjugate virtual machine, a binding trailer method, and an invocation method.

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9. (Original) A system to efficiently design and implement a matched instruction set processor system, including:

an application modeling unit to analyze and map design specifications of the matched instruction set processor into application components, each application component representing a reusable function commonly used in digital communication systems;

an architectural modeling unit operatively coupled to the application modeling unit, the architectural modeling unit decomposing the matched instruction set processor system into interconnected design vectors; and

a realization mapping unit operatively coupled to the architectural modeling unit, the realization mapping unit analyzing and mapping the interconnected design vectors into specific hardware and software elements.

10. (Original) The system of claim 9, wherein the application modeling unit performs a behavioral analysis of the matched instruction set processor system to ensure compliance with the design specifications.

11. (Original) The system of claim 9, wherein the application modeling unit performs a requirement analysis of the design specifications of the matched instruction set processor system to generate a behavioral model.

12. (Currently Amended) The system of claim 9, wherein the application modeling unit represents ~~[[the]]~~ a behavioral model using application components.

13. (Original) The system of claim 9, wherein the architectural modeling unit maps the application components into corresponding architectural components.

14. (Original) The system of claim 13, wherein the architectural modeling unit decomposes each application component into processing pipelines to satisfy system processing and timing requirements.

15. (Original) The system of claim 14, wherein the architectural modeling unit decomposes each processing pipeline into design vectors, including functional design vectors and interconnect design vectors.

16. (Currently Amended) The system of claim 15, wherein the architectural

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modeling unit uses the functional design vectors to represent design information for at least one functional aspect of the processing pipeline.

~~using the interconnect design vectors to contain connectivity characteristics of the processing pipeline.~~

17. (Currently Amended) The system of claim ~~[[15]]~~ 16, wherein the architectural modeling unit uses the interconnect design vectors to contain connectivity characteristics of the processing pipeline.

18. (Original) The system of claim 17, wherein the architectural modeling unit provides in each design vector a binding header method, a run method, a conjugate virtual machine, a binding trailer method, and an invocation method.

19. (Cancelled).

20. (New) The method of claim 1, wherein the interconnected design vectors are represented in Java programming language.

21. (New) The system of claim 9, wherein the design vectors are represented in Java programming language.